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EXAMINER	
MATISIAK, JENNIFER E	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/813,886	ZHANG ET AL.	
	Examiner	Art Unit	
	Jennifer Matisiak	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 10-31, 33-42* is/are rejected.

7)☒ Claim(s) *9 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05032004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claim 23 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant does not disclose the manner in which the computer-readable medium encodes an integrated circuit product.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 23 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant does not clarify whether the integrated circuit product or the computer-readable medium comprises the inductor and enclosure.

Claim Objections

3. Claims 9 and 32 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Regarding claims 9 and 32, the claim limitations broaden the scope of the parent claims rather than narrow the scope of claims 8 and 31 respectively.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 1000, 1002, 1004, 1006, 1008, 1010, 1016 and 1066. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 8, 10-11, 13-17, 24, 31 and 33-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Liou et al. (US 6037649), hereinafter Liou.

Regarding claim 1, Liou discloses an apparatus (Fig. 3C, for example) comprising: an inductor (M1 22, M2 25, M3 28, 21, 23, 26); and an electrically conductive enclosure (S1 31, S2 32, S3 33) electromagnetically shielding the inductor, the electrically conductive enclosure having an aperture (see figure below) at least as large as the inductor, the aperture being substantially centered around a projected surface of the inductor.

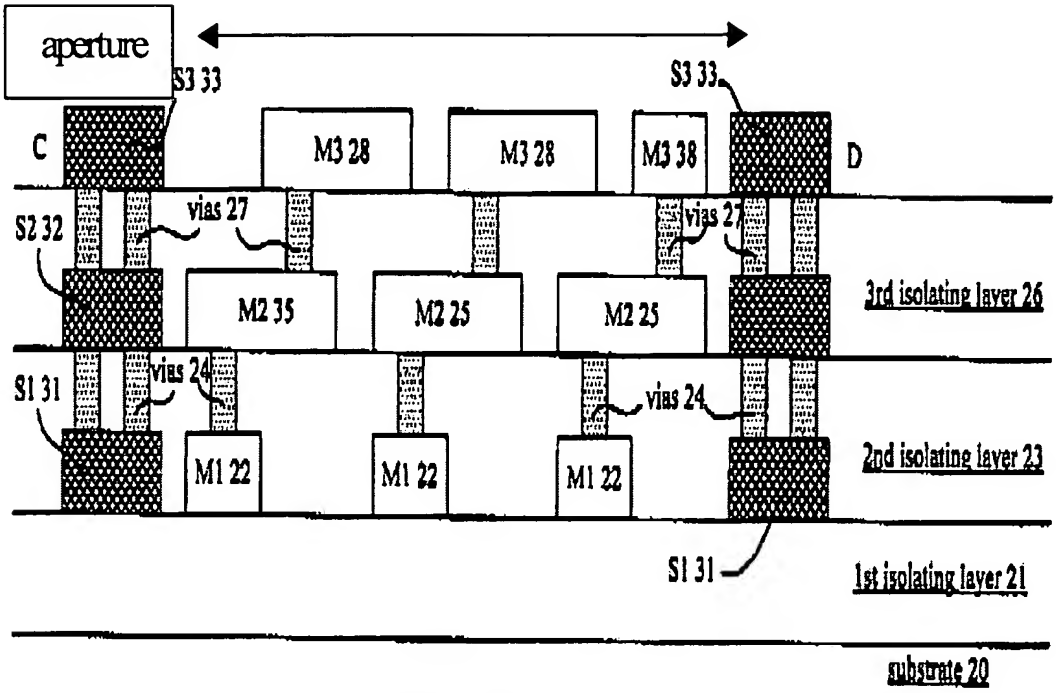

FIG. 3C

Regarding claim 2, Liou discloses an apparatus wherein the aperture is substantially parallel to a plane of current flow in the inductor (Fig. 3C).

Regarding claim 8, Liou discloses an apparatus (Fig. 3C) wherein the electrically conductive enclosure (S1 31, S2 32, S3 33) includes a top plate (S3 33), a bottom plate (S1 31), and sidewalls (S2 32).

Regarding claim 10, Liou discloses an apparatus (Fig. 3C) wherein the aperture is formed in the bottom plate (S1 31).

Regarding claim 11, Liou discloses an apparatus wherein the bottom plate (S1 31) is formed in one integrated circuit metal layer (col 4, lines 57-60).

Regarding claim 13, Liou discloses an apparatus (Fig. 3C) wherein the top plate (S3 33) is formed in a redistribution layer (see figure below, col 3, lines 59-62).

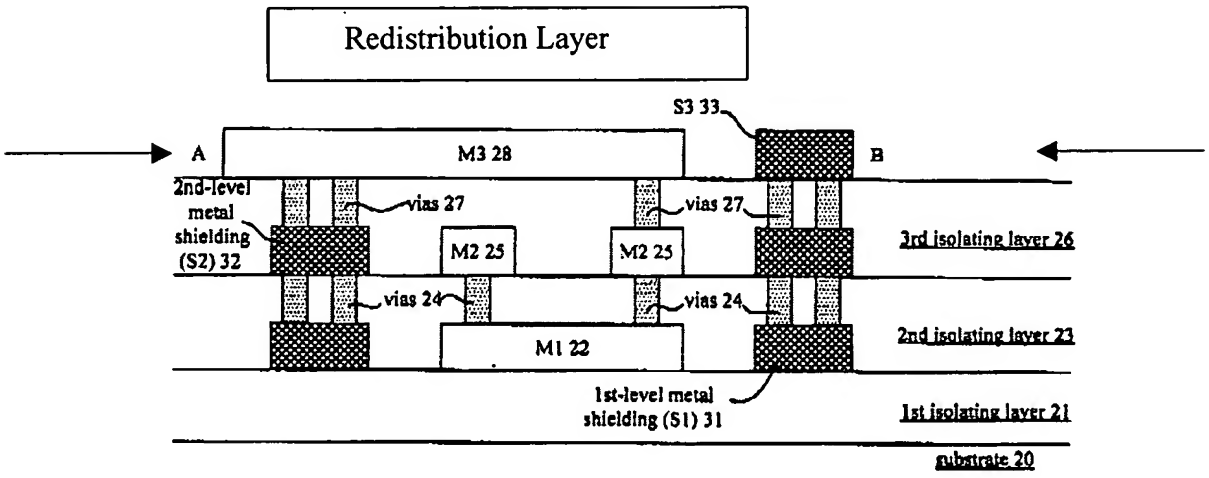

FIG. 3B

Regarding claim 14, Liou discloses an apparatus (Fig. 3C), wherein the top plate (S3 33) is formed in a package substrate (each layer comprises the substrate).

Regarding claim 15, Liou discloses an apparatus (Fig. 3C) wherein the inductor is formed at least partially in one or more metal layers (M1 22, M2 25, M3 28) of an integrated circuit die thicker than others of the metal layers (24, 27).

Regarding claim 16, Liou discloses an apparatus (Fig. 3C) wherein the inductor (M1 22, M2 25, M3 28, 21, 23, 26) is formed at least partially in one or more redistribution layers (see figure above) formed on an integrated circuit die.

Regarding claim 17, Liou discloses an apparatus (Fig. 3C) wherein the inductor is formed on an integrated circuit die (col 4, lines 16-17).

Regarding claim 24, Liou discloses a method of manufacturing an integrated circuit product (Fig. 3C) comprising: forming an inductor (col 2, lines 42-44); and forming an electrically conductive enclosure (col 4, lines 57-60) electromagnetically shielding the inductor, the electrically conductive enclosure having an aperture (as shown in figure above) at least as large as the inductor, the aperture being substantially centered around a projected surface of the inductor.

Regarding claim 31, Liou discloses a method (Fig. 3C) further comprising: forming the electrically conductive enclosure (S3 33, S2, 32, S1, 31, col 4, lines 57-60) including a top plate (S3 33), a bottom plate (S1 31), and sidewalls (S2 32).

Regarding claim 33, Liou discloses a method further comprising: forming the aperture in the bottom plate (Fig. 3C).

Regarding claim 34, Liou discloses a method (Fig. 3C) further comprising: forming one or more integrated circuit metal layers on an integrated circuit die; and forming the bottom plate in the one or more integrated circuit metal layers (col 4, lines 57-60).

Regarding claim 35, Liou discloses a method (Fig. 3C) further comprising: forming a metal (M1, M2, M3) on an integrated circuit die; and forming the top plate (S3 33) in the metal layer (col 4, lines 57-60).

Regarding claim 36, Liou discloses a method (Fig. 3C, col 2, lines 24-28) further comprising: forming a redistribution layer (as shown in figure above) on an integrated circuit die; and forming the top plate (S3 33) in the redistribution layer.

Regarding claim 37, Liou discloses a method (Fig. 3C, col 2, lines 24-28) further comprising: forming a package substrate (20); and forming the top plate (S3 33) in the package substrate.

Regarding claim 38, Liou discloses a method (Fig. 3C, col 2, lines 24-28) further comprising: forming one or more metal layers (M1, M2, M3) on an integrated circuit die thicker than others of the metal layers (24, 27); and forming the inductor (M3 28, M2 25, M1 22, 21, 23, 26) at least partially in the one or more metal layers.

Regarding claim 39, Liou discloses a method (Fig. 3C, col 2, lines 24-28) further comprising: forming redistribution layers (as shown in figure above) on an integrated circuit die; and forming the inductor (M3 28, M2 25, M1 22) at least partially in one or more redistribution layers.

6. Claims 1, 3-5, 7, 20-22, 24, 26-28 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Acosta et al. (US 2002/0109204), hereinafter Acosta.

Regarding claim 1, Acosta discloses an apparatus (Fig. 7, for example) comprising: an inductor (5); and an electrically conductive enclosure (2) electromagnetically shielding the inductor, the electrically conductive enclosure having an aperture (1 of Fig. 2B, for example) at least as large as the inductor, the aperture being substantially centered around a projected surface of the inductor.

Regarding claim 3, Acosta discloses an apparatus (Fig. 7) wherein the aperture (1 of Fig. 2B) has an approximate diameter determined by adding an approximate outer diameter of the inductor to an approximate inner diameter of the inductor (5). Although not explicit in the written disclosure, it can be clearly shown from Fig. 7 that the diameter as measured across the diagonal length of the bottom of the well and the diameter as measured across the diagonal length of the top of the well correspond respectively to the inner and outer diameter of the inductor.

Regarding claim 4, Acosta discloses an apparatus (Fig. 7) further comprising: one or more electrically conductive links (9 of Fig. 3A, for example) extending across the aperture (1 of Fig. 2B) and electrically coupled to the electrically conductive enclosure (3 of Fig. 7), the electrically conductive links reducing an effect of electromagnetic signals external to the electrically conductive enclosure on the inductor (see abstract).

Regarding claim 5, Acosta discloses an apparatus, as recited in claim 4, wherein the electrically conductive links (9 of Fig. 3A) reduce coupling in the inductor from external sources. Acosta does not explicitly recite "wherein the electrically conductive links reduce coupling in the inductor from external sources by approximately 6dB." However, since the invention taught by Acosta is identical to the claimed invention, it inherently performs the claimed function.

Regarding claim 7, Acosta discloses an apparatus (Fig. 7) wherein the electrically conductive links (9 of Fig. 3A) are formed in the one traditional integrated circuit layer (para [0030]).

Regarding claim 20, Acosta discloses a method (Figs. 2A,B, 3A,B, 4A,B, 5-7) comprising: reducing a current induced (para [0019]) in an electrically conductive enclosure (3 of Fig. 7) generated in response to an inductor (5), the induced current generating an electromagnetic field counteracting an effective electromagnetic field generated by the inductor, the reducing using at least one aperture (1 of Fig. 2B) in the electrically conductive enclosure.

Regarding claim 21, Acosta discloses a method (Figs. 2A,B, 3A,B, 4A,B, 5-7) further comprising: reducing an effective aperture (1 of Fig. 2B) utilizing links (9 of Fig. 3A) for generating a current to counteract at least some external electromagnetic signals (para [0031]) entering the electrically conductive enclosure (3 of Fig. 7) through the aperture.

Regarding claim 22, Acosta discloses a method (Figs. 2A,B, 3A,B, 4A,B, 5-7) further comprising: providing the inductor (5 of Fig. 7) on the integrated circuit die (para [0030]) with sufficient space (para [0033]) with respect to the electrically conductive enclosure (3 of Fig. 7) to reduce the current induced in the electrically conductive enclosure (para [0019]).

Regarding claim 24, Acosta discloses a method of manufacturing an integrated circuit product (Figs. 2A,B, 3A,B, 4A,B, 5-7) comprising: forming an inductor (5 of Fig. 7); and forming an electrically conductive enclosure (3 of Fig. 7) electromagnetically shielding the inductor, the electrically conductive enclosure having an aperture (1 of Fig. 2B) at least as large as the inductor, the aperture being substantially centered around a projected surface of the inductor.

Regarding claim 26, Acosta discloses a method (Figs. 2A,B, 3A,B, 4A,B, 5-7) further comprising: forming the aperture (1 of Fig. 2B) having an approximate diameter determined by adding an approximate outer diameter of the inductor (5 of Fig.7) to an approximate inner diameter of the inductor. Although not explicit in the written disclosure, it can be clearly shown from Fig. 7 that the diameter as measured across the diagonal length of the bottom of the well and the diameter as measured across the diagonal length of the top of the well correspond respectively to the inner and outer diameter of the inductor.

Regarding claim 27, Acosta discloses a method (Figs. 2A,B, 3A,B, 4A,B, 5-7) further comprising: forming one or more electrically conductive links (9 of Fig. 3A) extending across the aperture (1 of Fig. 2B) and electrically coupled to the electrically conductive enclosure (3 of Fig. 7), the electrically conductive links reducing an effect of electromagnetic signals (para [0019]) external to the electrically conductive enclosure on the inductor (5).

Regarding claim 28, Acosta discloses a method (Figs. 2A,B, 3A,B, 4A,B, 5-7) wherein the electrically conductive links (9 of Fig. 3A) reduce coupling in the inductor (5 of Fig.7) from external sources. Acosta does not explicitly disclose "by approximately 6dB." However, because the invention of Acosta is identical to the claimed invention, it inherently performs the claimed function.

Regarding claim 30, Acosta discloses a method (Figs. 2A,B, 3A,B, 4A,B, 5-7); further comprising forming the electrically conductive links (9 of Fig. 3A) in the one or more traditional integrated circuit layers (para [0030]).

7. Claims 1, 2, 8, 12, 20, 23-25, 31 and 42 are rejected under 35 U.S.C. 102(e) as being anticipated by Wolf et al. (US 6653557), hereinafter Wolf.

Regarding claim 1, Wolf discloses an apparatus (Fig. 8A) comprising: an inductor (1118 of Fig. 22A); and an electrically conductive enclosure (840 of Fig. 8A; see abstract) electromagnetically shielding the inductor, the electrically conductive enclosure having an aperture (area enclosed by 208) at least as large as the inductor, the aperture being substantially centered around a projected surface of the inductor.

Regarding claim 2, Wolf discloses an apparatus (Fig. 8A) wherein the aperture (area enclosed by 208) is substantially parallel (Fig. 22A) to a plane of current flow in the inductor.

Regarding claim 8, Wolf discloses an apparatus, as recited in claim 1, wherein the electrically conductive enclosure includes a top plate (206 of Fig. 7), a bottom plate (170 of Fig. 8A), and sidewalls (208, col 3, lines 36-38).

Regarding claim 12, Wolf discloses an apparatus (Fig. 8A) wherein the top plate (206 of Fig. 7) is formed in a metal layer (col 14, lines 57-59).

Regarding claim 20, Wolf discloses a method (col 3, lines 13-21) comprising: reducing a current induced in an electrically conductive enclosure (col 3, lines 1-3) generated in response to an inductor (col 1, lines 20-24), the induced current generating an electromagnetic field counteracting an effective electromagnetic field generated by the inductor, the reducing using at least one aperture (col 2, lines 66-67; col 3, line1) in the electrically conductive enclosure.

Regarding claim 23, Wolf discloses a computer-readable medium (104 of Fig. 1, for example) encoding an integrated circuit product (122 of Fig. 7, for example) comprising: an inductor (1118 of Fig. 22A); and an electrically conductive enclosure (840 of Fig. 8A) electromagnetically shielding the inductor, the electrically conductive enclosure having an aperture (area enclosed by 208) at least as large as the inductor, the aperture being substantially centered around a projected surface of the circuit element.

Regarding claim 24, Wolf discloses a method of manufacturing (col 3, lines 13-21) an integrated circuit product (Fig. 8A) comprising: forming an inductor (1118 of Fig. 22A); and forming an electrically conductive enclosure (col 14 lines 57-59) electromagnetically shielding the inductor, the electrically conductive enclosure having an aperture (area enclosed by sidewalls 208) at least as large as the inductor, the aperture being substantially centered around a projected surface of the inductor.

Regarding claim 25, Wolf discloses a method (Fig. 8A, col 3, lines 13-21) further comprising: forming the aperture substantially parallel to a plane of current flow in the inductor (Fig. 22A).

Regarding claim 31, Wolf discloses a method (Fig. 8A, col 3, lines 13-21) further comprising: forming the electrically conductive enclosure (840) including a top plate (206 of Fig. 7, col 14, lines 57-59), a bottom plate (170 of Fig. 8A, col 14, lines 57-59), and sidewalls (208, col 3, lines 36-38).

Regarding claim 42, Wolf discloses an apparatus (Fig. 8A) comprising: means for electrically coupling nodes of an integrated circuit (col 11, lines 11-16); means for

electromagnetically shielding the coupling means (840 of Fig. 8A); and means for reducing current induced in the shielding means in response to the coupling means (col 3, lines 1-3), the induced current generating an electromagnetic field counteracting an electromagnetic field generated by the coupling means.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liou.

Regarding claim 18, Liou discloses an apparatus (Fig. 3C) wherein a conductor (M1 22, M2 25, M3 28) is forming the inductor (M1 22, M2 25, M3 28, 21, 23, 26). Liou does not explicitly recite is "10 um wide." However:

> "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Therefore it would have been obvious to one of ordinary skill in the art to arrive at the optimal value through routine experimentation since it is desirable to make the invention of Liou electrically and structurally sound.

Regarding claim 19, Liou discloses an apparatus (Fig. 3C) as recited in claim 17. Liou does not explicitly recite "wherein the aperture and the inductor are effectively spaced at least 10.25 micrometers apart." However, for the reasons disclosed above, it would have been obvious to one of ordinary skill in the art to arrive at the optimal value through routine experimentation since it is desirable to make the invention of Liou electrically and structurally sound.

9. Claims 6, 29, 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Acosta.

Regarding claim 6, Acosta discloses an apparatus (Fig. 7) as recited in claim 4. Acosta does not explicitly disclose "wherein the electrically conductive links are approximately 5 micrometers wide." However:

> "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Therefore it would have been obvious to one of ordinary skill in the art to arrive at the optimal value through routine experimentation since it is desirable to make the invention of Acosta electrically and structurally sound.

Regarding claim 29, Acosta discloses a method (Figs. 2A,B, 3A,B, 4A,B, 5-7) further comprising forming electrically conductive links (9 of Fig. 3A). Acosta does not explicitly disclose "approximately 5 micrometers wide." However, it would have been obvious to one of ordinary skill in the art to arrive at the optimal value through routine experimentation, as discussed above, since it is desirable to make the invention of Acosta electrically and structurally sound.

Regarding claim 40, Acosta discloses a method (Figs. 2A,B, 3A,B, 4A,B, 5-7) further comprising: forming the inductor (5 of Fig. 7) using a conductor. Acosta does not explicitly disclose "that is 10 micrometers wide." However, it would have been obvious to one of ordinary skill in the art to arrive at the optimal value through routine experimentation, as discussed above, since it is desirable to make the invention of Acosta electrically and structurally sound.

Regarding claim 41, Acosta discloses a method (Figs. 2A,B, 3A,B, 4A,B, 5-7) further comprising: forming the aperture (1 of Fig. 2B) effectively spaced from the inductor (5 of Fig. 7). Acosta does not explicitly disclose "by at least 10.25 micrometers." However, for the reasons disclosed above, it would have been obvious to one of ordinary skill in the art to arrive at the optimal value through routine experimentation since it is desirable to make the invention of Acosta electrically and structurally sound.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer Matisiak whose telephone number is 571-272-2639. The examiner can normally be reached on Business Days 9:30a-6:30p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 517-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEM

DOUGLAS W. OWENS
PRIMARY EXAMINER